CLAIMS

1. A method for limiting a pulse width in a chip clock design of a circuit, the circuit receiving a clock signal having a clock pulse width, the method comprising the steps of:

detecting the clock pulse width of the clock signal;

determining whether the clock pulse width is larger than a maximum clock pulse width; and

upon a determination that the clock pulse width is larger than a maximum clock pulse width, limiting the clock pulse width of the clock signal.

2. The method of Claim 1, wherein the clock pulse width is limited to the maximum clock pulse width.

3. The method of Claim 1, further comprising the step of, upon a determination that the clock pulse width is smaller than or equal to the maximum clock pulse width, relaying the clock pulse to the circuit without changing the clock pulse width.

4. The method of Claim 1, further comprising the step of preventing the circuit from being exposed to testing environments for an excessively long period of time, thereby limiting exposure of the circuit to the testing environments.

5. The method of Claim 1, further comprising the step of determining a maximum clock pulse width for the clock signal.

6. The method of Claim 1, wherein the circuit comprises a dynamic circuit having one or more dynamic nodes.

7. An apparatus for limiting a pulse width in a chip clock design of a circuit, the circuit receiving a clock signal having a clock pulse width, the apparatus comprising:

means for detecting the clock pulse width of the clock signal;

means for determining whether the clock pulse width is larger than a maximum clock pulse width; and

means for, upon a determination that the clock pulse width is larger than a maximum clock pulse width, limiting the clock pulse width of the clock signal.

8. The apparatus of Claim 7, wherein the clock pulse width is limited to the maximum clock pulse width.

9. The apparatus of Claim 7, further comprising means for, upon a determination that the clock pulse width is smaller than or equal to the maximum clock pulse width, relaying the clock pulse to the circuit without changing the clock pulse width.

10. The apparatus of Claim 7, further comprising means for preventing the circuit from being exposed to testing environments for an excessively long period of time, thereby limiting exposure of the circuit to the testing environments.

11. The apparatus of Claim 7, further comprising means for determining a maximum clock pulse width for the clock

signal.

12. The apparatus of Claim 7, wherein the circuit comprises a dynamic circuit having one or more dynamic nodes.

13. A computer program product for limiting a pulse width in a chip clock design of a circuit, the circuit receiving a clock signal having a clock pulse width, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer program code for detecting the clock pulse width of the clock signal;

computer program code for determining whether the clock pulse width is larger than a maximum clock pulse width; and

computer program code for, upon a determination that the clock pulse width is larger than a maximum clock pulse width, limiting the clock pulse width of the clock signal.

14. The computer program product of Claim 13, wherein the clock pulse width is limited to the maximum clock pulse width.

15. The computer program product of Claim 13, the computer program further comprising computer program code for, upon a determination that the clock pulse width is smaller than or equal to the maximum clock pulse width, relaying the clock pulse to the circuit without changing the clock pulse width.

16. The computer program product of Claim 13, the computer program further comprising computer program code for preventing the circuit from being exposed to testing environments for an excessively long period of time, thereby limiting exposure of the circuit to the testing environments.

17. The computer program product of Claim 13, the computer program further comprising computer program code for determining a maximum clock pulse width for the clock signal.

18. The computer program product of Claim 13, wherein the circuit comprises a dynamic circuit having one or more dynamic nodes.

19. An apparatus for limiting a pulse width in a chip clock design of a circuit, the circuit receiving a clock signal having a clock pulse width, the apparatus comprising:

a phase-locked loop (PLL) for generating the clock signal;

a pulse-limiting circuit coupled to the PLL for automatically limiting the clock pulse width, if the clock pulse width is larger than the maximum clock pulse width;

a switch coupled to both the PLL and the pulse-limiting circuit; and

an override signal coupled to the switch for bypassing the pulse-limiting circuit.